



MOTOROLA
Semiconductor Products Sector

Order Number: MPC7410PEPNS/D
Rev. 0, 10/2001

Motorola Part Numbers Affected:
XPC7410RX450PE
XPC7410RX500PE
XPC7410RX550PE

PowerPC™

MPC7410 Part Number Specification for the RXxxxPE Series

This document describes part-number-specific changes to recommended operating conditions and revised electrical specifications, as applicable, from those described in the general *MPC7410 Hardware Specifications* (order # MPC7410EC/D).

Specifications provided in this document supersede those in the *MPC7410 Hardware Specifications* for the part numbers listed in Table A only. Specifications not addressed herein are unchanged. Because this document is frequently updated, refer to <http://www.motorola.com/sps> or to your Motorola sales office for the latest version.

Note that headings and table numbers in this document are not consecutively numbered. They are intended to correspond to the heading or table affected in the general hardware specification.

Part numbers addressed in this document are listed in Table A. For more detailed ordering information see Table B.

This document contains information on a new product under development by Motorola.
Motorola reserves the right to change or discontinue this product without notice.

© Motorola, Inc., 2001. All rights reserved.

 **Digital DNA**
From Motorola

PRELIMINARY—SUBJECT TO CHANGE WITHOUT NOTICE

Features

Table A. Part Numbers Addressed by this Data Sheet

| Motorola Part Number | Operating Conditions | | | Significant Differences from Hardware Specification |
|----------------------|----------------------|-----------|---------------------|--|
| | CPU Frequency | Vdd | T _J (°C) | |
| XPC7410RX450PE | 450 MHz | 2.0V±50mV | 0 to 65 | Modified voltage and temperature specification to achieve 450Mhz frequency |
| XPC7410RX500PE | 500 MHz | 2.0V±50mV | 0 to 65 | Modified voltage and temperature specification to achieve 500Mhz frequency |
| XPC7410RX550PE | 550 MHz | 2.0V±50mV | 0 to 65 | Modified voltage and temperature specification to achieve 550Mhz frequency |

Note: The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.2 Features

This section summarizes changes to the features of the MPC7410 described in the MPC7410 Hardware Specifications.

1.4.1 DC Electrical Characteristics

Table 3 provides the recommended operating conditions for the MPC7410 part numbers described herein.

Table 3. Recommended Operating Conditions

| Characteristic | | Symbol | Recommended Value | Unit |
|------------------------------|-------------------------------------|--------|-------------------|------|
| Core supply voltage | | Vdd | 2.0V ± 50mV | V |
| PLL supply voltage | | AVdd | 2.0V ± 50mV | V |
| L2 DLL supply voltage | | L2AVdd | 2.0V ± 50mV | V |
| Processor bus supply voltage | BVSEL = 1 or BVSEL = HRESET | OVdd | 3.3 ± 165mV | |
| | BVSEL = $\overline{\text{HRESET}}$ | OVdd | 2.5V ± 125mV | V |
| | BVSEL = GND | OVdd | 1.8V ± 90mV | V |
| L2 bus supply voltage | L2VSEL = $\overline{\text{HRESET}}$ | L2OVdd | 2.5V ± 125mV | V |
| | L2VSEL = GND | L2OVdd | 1.8V ± 90mV | V |

Table 3. Recommended Operating Conditions (Continued)

| Characteristic | | Symbol | Recommended Value | Unit |
|--------------------------|---------------|----------|-------------------|------|
| Input voltage | Processor bus | V_{in} | GND to OVdd | V |
| | L2 Bus | V_{in} | GND to L2OVdd | V |
| | JTAG Signals | V_{in} | GND to OVdd | V |
| Die-junction temperature | | T_j | 0-65 | °C |

Note:

These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 7 provides the power consumption of the MPC7410 part at the frequencies described herein.

Table 7. Power Consumption for MPC7410

| | Processor (CPU) Frequency | Processor (CPU) Frequency | Processor (CPU) Frequency | Unit | Notes |
|---------------------------------|---------------------------|---------------------------|---------------------------|------|-------|
| | 450Mhz | 500Mhz | 550Mhz | | |
| Full-On Mode | | | | | |
| Typical | 5.9 | 6.5 | 7.1 | W | 1, 3 |
| Maximum | 13.2 | 14.7 | 16.2 | W | 1, 2 |
| Doze Mode | | | | | |
| Maximum | 4.5 | 5 | 5.5 | W | 1, 2 |
| Nap Mode | | | | | |
| Maximum | 2.13 | 2.25 | 2.37 | W | 1, 2 |
| Sleep Mode | | | | | |
| Maximum | 2.13 | 2.25 | 2.37 | W | 1, 2 |
| Sleep Mode—PLL and DLL Disabled | | | | | |
| Typical | 0.5 | 0.5 | 0.5 | W | 1, 3 |
| Maximum | 2.0 | 2.0 | 2.0 | W | 1, 2 |

Notes:

1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system-dependent, but is typically <10% of Vdd power. Worst-case power consumption for AVdd = 15 mw and L2AVdd = 15 mW.
2. Maximum power is measured at 65 °C and Vdd = 2.0V while running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including Altivec, maximally busy.
3. Typical power is an average value measured at 65 °C and Vdd = 2.0V in a system while running typical benchmarks.

Features

1.4.2.1 Clock AC Specifications

Table 8 provides the additional clock AC timing specifications described in this document. Refer to the *MPC7410 Hardware Specification* for the remaining frequencies.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (See Table 3)

| Characteristic | Symbol | 450 MHz | | 500 MHz | | 550 MHz | | Unit | Notes |
|--|-------------------------------------|---------|-----------|---------|-----------|---------|-----------|---------------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| Processor frequency | f_{core} | 300 | 450 | 300 | 500 | 300 | 550 | MHz | |
| VCO frequency | f_{VCO} | 600 | 900 | 600 | 1000 | 600 | 1100 | MHz | |
| SYSCLK frequency | f_{SYSCLK} | 33 | 133 | 33 | 133 | 33 | 133 | MHz | 1 |
| SYSCLK cycle time | t_{SYSCLK} | 7.5 | 30 | 7.5 | 30 | 7.5 | 30 | ns | |
| SYSCLK rise and fall time | t_{KR} | — | 1.0 | — | 1.0 | — | 1.0 | ns | 2 |
| | t_{KF} | — | 0.5 | — | 0.5 | — | 0.5 | ns | 3 |
| SYSCLK duty cycle measured at $OV_{\text{dd}}/2$ | $t_{\text{KHKL}}/t_{\text{SYSCLK}}$ | 40 | 60 | 40 | 60 | 40 | 60 | % | 4 |
| SYSCLK jitter | | — | ± 150 | — | ± 150 | — | ± 150 | ps | 5 |
| Internal PLL relock time | | — | 100 | — | 100 | — | 100 | μs | 6 |

Note:

See general hardware specification.

1.4.2.2 Processor Bus AC Specifications

Table 9 provides processor bus AC timing specifications for the MPC7410 part described in this document.

Table 9. Processor Bus AC Timing Specifications

At $V_{dd}=AV_{dd}=2.0V\pm 50mV$; $0 \leq T_j \leq 65^\circ C$, $OV_{dd} = 2.5V\pm 0.125V$ and $OV_{dd} = 1.8V\pm 0.090V$, 60X bus at 133MHz

| Parameter | Symbol | 450, 500, 550 Mhz | | Unit | Notes |
|---|-------------|-------------------|-----|--------------|---------|
| | | Min | Max | | |
| Mode select input setup to HRESET | t_{MVRH} | 8 | — | t_{sysclk} | 2,3,4,5 |
| HRESET to mode select input hold | t_{MXRH} | 0 | — | ns | 2,3,5 |
| Setup Times: | | | | ns | 10 |
| Address/Transfer Attribute | t_{AVKH} | 1.4 | — | | 6 |
| Transfer Start (TS) | t_{TSVKH} | 1.4 | — | | — |
| Data/Data Parity | t_{DVKH} | 1.4 | — | | 7 |
| ARTRY/SHD0/SHD1 | t_{ARVKH} | 1.4 | — | | — |
| All Other Inputs | t_{IVKH} | 1.4 | — | | 8 |
| Input Hold Times: | | | | ns | 11 |
| Address/Transfer Attribute | t_{AXKH} | 0 | — | | 6 |
| Transfer Start (TS) | t_{TSXKH} | 0 | — | | — |
| Data/Data Parity | t_{DXKH} | 0 | — | | 7 |
| ARTRY/SHD0/SHD1 | t_{ARXKH} | 0 | — | | — |
| All Other Inputs | t_{IXKH} | 0 | — | | 8 |
| Valid Times: | | | | ns | 12 |
| Address/Transfer Attribute | t_{KHAV} | — | 3.0 | | 6 |
| TS, ABB, DBB | t_{KHTSV} | — | 3.0 | | — |
| Data | t_{KHdV} | — | 3.5 | | 7 |
| Data Parity | t_{KHdPV} | — | 3.5 | | 7 |
| ARTRY/SHD0/SHD1 | t_{KHARV} | — | 2.3 | | — |
| All Other Outputs | t_{KHOV} | — | 3.0 | | 9 |
| Output Hold Times: | | | | ns | 13 |
| Address/Transfer Attribute | t_{KHAX} | 0.75 | — | | 6 |
| TS, ABB, DBB | t_{KHtSX} | 0.75 | — | | — |
| Data/Data Parity | t_{KHdX} | 0.6 | — | | 7 |
| ARTRY/SHD0/SHD1 | t_{KHARX} | 0.75 | — | | — |
| All Other Outputs | t_{KHOX} | 0.75 | — | | 9 |
| SYSCLK to Output Enable | t_{KHOE} | 0.5 | — | ns | 14 |
| SYSCLK to Output High Impedance (all except TS, ABB/AMON(0), ARTRY/SHD, DBB/DMON(0)) | t_{KHOZ} | — | 3.5 | ns | 15 |

Features

Table 9. Processor Bus AC Timing Specifications (Continued)

At $V_{dd}=AV_{dd}=2.0V\pm 50mV$; $0 \leq T_j \leq 65^\circ C$, $OV_{dd} = 2.5V \pm 0.125V$ and $OV_{dd} = 1.8V \pm 0.090V$, 60X bus at 133MHz

| Parameter | Symbol | 450, 500, 550 Mhz | | Unit | Notes |
|--|--------------|-------------------|-----|--------------|------------|
| | | Min | Max | | |
| SYSCLK to \overline{TS} , $\overline{ABB/AMON}(0)$, $\overline{DBB/DMON}(0)$ High Impedance after precharge | t_{KHABPZ} | — | 1.0 | t_{sysclk} | 4,15,16,17 |
| Maximum Delay to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ Precharge | t_{KHARP} | — | 1 | t_{sysclk} | 4,17 |
| SYSCLK to $\overline{ARTRY}/\overline{SHD0}/\overline{SHD1}$ High Impedance After Precharge | t_{KHARPZ} | — | 2 | t_{sysclk} | 4,17 |

Note:

See general hardware specification.

1.4.2.3 L2 Clock AC Specifications

Table 10 provides L2CLK output AC timing specifications for the MPC7410 part described in this document.

Table 10. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3)

| Parameter | Symbol | 450 MHz | | 500 MHz | | 550 MHz | | Unit | Notes |
|--------------------------|----------------------|---------|-----------|---------|-----------|---------|-----------|-------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| L2CLK frequency | f_{L2CLK} | 150 | 225 | 150 | 250 | 150 | 275 | MHz | 1 |
| L2CLK cycle time | t_{L2CLK} | 4.4 | 6.67 | 4.0 | 6.67 | 3.64 | 6.67 | ns | |
| L2CLK duty cycle | t_{CHCL}/t_{L2CLK} | 50 | | 50 | | 50 | | % | 2 |
| Internal DLL-relock time | | 640 | — | 640 | — | 640 | — | L2CLK | 4 |
| DLL capture window | | | ± 200 | | ± 200 | | ± 200 | ns | 5 |

Note:

See general hardware specification.

1.4.2.4 L2 Bus AC Specifications

Table 11 provides the L2 Bus Interface AC Timing Specifications for the frequencies described in this document.

Table 11. L2 Bus Interface AC Timing Specifications

At $V_{dd}=AV_{dd}=L2AV_{dd}=2.05V\pm 50mV$; $0\leq T_j\leq 65^\circ C$, $L2OV_{dd}=2.5V\pm 0.125V$ and $L2OV_{dd}=1.8V\pm 0.090V$

| Parameter | Symbol | 450, 500, 550 MHz | | Unit | Notes |
|--|-------------------------|--------------------------|------------------------------|------|-------|
| | | Min | Max | | |
| L2SYNC_IN rise and fall time | t_{L2CR} & t_{L2CF} | — | 1.0 | ns | 1 |
| Setup Times: Data and parity | t_{DVL2CH} | 1.250 | — | ns | 2 |
| Input Hold Times: Data and parity | t_{DXL2CH} | — | 0.0 | ns | 2 |
| Valid Times: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11 | t_{L2CHOV} | - - - - | 2.25 2.50 2.75 3.25 | ns | 3,4 |
| Output Hold Times All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11 | t_{L2CHOX} | 0.5 0.9 1.3 1.7 | - - - - | ns | 3 |
| L2SYNC_IN to high impedance: All outputs when L2CR[14-15] = 00 All outputs when L2CR[14-15] = 01 All outputs when L2CR[14-15] = 10 All outputs when L2CR[14-15] = 11 | t_{L2CHOZ} | - - - - | 2.0 2.5 3.0 3.5 | ns | |

Note:

See general hardware specification

1.10 Ordering Information

This section regards part numbers and markings.

1.10.1 Part Numbers Addressed by this Specification

Table B provides ordering information for the MPC7410 part described in this document.

Ordering Information

Table B. Part-Marking Nomenclature

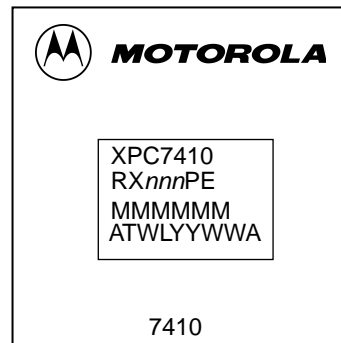
| XPC | 7450 | RX | xxx | x | x |
|------------------|-----------------|-----------|----------------------------------|--------------------------------|-------------------------|
| Product Code | Part Identifier | Package | Processor Frequency ¹ | Application Modifier | Revision Level |
| XPC ² | 7410 | RX = CBGA | 450 500 550 | P: 2.0 V ± 50 mV 0 to 65° C | E: 1.4; PVR = 800C 1104 |

Notes:

1. Processor core frequencies supported by parts addressed by this specification only. Parts addressed by other specifications may support other maximum core frequencies.
2. The X prefix in a Motorola PowerPC part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.

1.10.2 Part Marking

Parts are marked as shown in Figure A.



Notes:

- nnn* is the speed grade of the part
- MMMMMM is the 6-digit mask number
- ATWLYYWWA is the traceability code
- CCCC is the country of assembly (this space is left blank if parts are assembled in the United States)

Figure A. Motorola Part Marking for BGA Device

Table C. Document History

| Revision Number | Changes |
|-----------------|-----------------|
| Rev 0 | Initial release |


Ordering Information



DigitalDNA is a trademark of Motorola, Inc.

The PowerPC name, the PowerPC logotype, and PowerPC 603e are trademarks of International Business Machines Corporation used by Motorola under license from International Business Machines Corporation.

Information in this document is provided solely to enable system and software implementers to use PowerPC microprocessors. There are no express or implied copyright licenses granted hereunder to design or fabricate PowerPC integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

TECHNICAL INFORMATION CENTER: 1-800-521-6274

HOME PAGE: <http://www.motorola.com/semiconductors>

DOCUMENT COMMENTS: FAX (512) 933-2625, Attn: RISC Applications Engineering

WORLD WIDE WEB ADDRESSES:

<http://www.motorola.com/PowerPC>

<http://www.motorola.com/NetComm>

<http://www.motorola.com/ColdFire>

MPC7410PEPNS/D



MOTOROLA